40-42 are configured to sense radiation (or radiation waves), such as an incident light 43, that is projected toward device substrate 32 from the back side 36. The light 43 would enter the device substrate 32 through the back side 36 (or the back surface) and be detected by one or more of the pixels 40-42. The pixels 40-42 each include a photodiode in the present embodiment. In other embodiments, the pixels 40-42 may include pinned layer photodiodes, photogates, reset transistors, source follower transistors, and transfer transistors. The pixels 40-42 may also be referred to as radiation-detection devices or light-sensors.

The pixels 40-42 may be varied from one another to have different junction depths, thicknesses, widths, and so forth. For the sake of simplicity, only three pixels 40-42 are illustrated in FIG. 1, but it is understood that any number of pixels may be implemented in the device substrate 32. In the embodiment shown, the pixels 40-42 are formed by performing an implantation process 46 on the device substrate 32 from the front side 34. The implantation process 46 includes doping the device substrate 32 with a p-type dopant such as boron. In an alternative embodiment, the implantation process 46 may include doping the device substrate 32 with an n-type dopant such as phosphorous or arsenic. In other embodiments, the pixels 40-42 may also be formed by a diffusion process.

The pixels 40-42 are separated from one another by a plurality of gaps in the device substrate 32. For example, a gap 45 separates the pixel 40 from an adjacent pixel to its left (not illustrated), a gap 46 separates the pixels 40-41, and a gap 47 separates the pixels 41-42. Of course, it is understood that the gaps 45-47 are not voids or open spaces in the device substrate 32, but they may be regions of the device substrate 32 (either a semiconductor material or a dielectric isolation element) that are located between the adjacent pixels 40-42.

Still referring to FIG. 1, the pixels 40-42 are formed in a region of the image sensor device 30 referred to as a pixel region 52 (or a pixel-array region). In addition to the pixel region 52, the image sensor 30 may also include a periphery region 54 and a bonding pad region 56. The dashed lines in FIG. 1 designate the approximate boundaries between the regions 52, 54, and 56, though it is understood that these regions 52, 54, and 56 are not drawn in scale herein and may extend vertically above and below the device substrate 32.

The periphery region 54 includes devices 60 and 61 that need to be kept optically dark. For example, the device 60 in the present embodiment may be a digital device, such as an application-specific integrated circuit (ASIC) device or a system-on-chip (SOC) device. The device 61 may be a reference pixel that is used to establish a baseline of an intensity of light for the image sensor device 30.

The bonding pad region 56 includes a region where one or more bonding pads (not illustrated herein) of the image sensor device 30 will be formed in a later processing stage, so that electrical connections between the image sensor device 30 and external devices may be established. Among other things, the bonding pad region 56 may contain an isolation structure, such as a shallow trench isolation (STI) 58. The STI 58 partially extends into the periphery region 54. One function of the STI 58 is that it helps insulate the silicon of the device substrate 32 from a conductive pad to be formed in the bonding pad region 56, which will be discussed below in more detail.

Although not illustrated herein for reasons of simplicity, it is understood that the image sensor 30 may also include a scribe line region. The scribe line region includes a region that separates one semiconductor die (for example, a semiconductor die that includes the bonding pad region 56, the periphery region 54, and the pixel region 52) from an adjacent semiconductor die (not illustrated). The scribe line region is cut therethrough in a later fabrication process to separate adjacent dies before the dies are packaged and sold as integrated circuit chips. The scribe line region is cut in such a way that the semiconductor devices in each die are not damaged.

Referring now to FIG. 2, an interconnect structure 65 is formed over the front side 34 of the device substrate 32. The interconnect structure 65 includes a plurality of patterned dielectric layers and conductive layers that provide interconnections (e.g., wiring) between the various doped features, circuitry, and input/output of the image sensor device 30. The interconnect structure 65 includes an interlayer dielectric (ILD) and a multilayer interconnect (MLI) structure. The MLI structure includes contacts, vias and metal lines. For purposes of illustration, a plurality of conductive lines 66 and vias/contacts 68 are shown in FIG. 2, it being understood that the conductive lines 66 and vias/contacts 68 illustrated are merely exemplary, and the actual positioning and configuration of the conductive lines 66 and vias/contacts 68 may vary depending on design needs.

The MLI structure may include conductive materials such as aluminum, aluminum/silicon/copper alloy, titanium, titanium nitride, tungsten, polysilicon, metal silicide, or combinations thereof, being referred to as aluminum interconnects. Aluminum interconnects may be formed by a process including physical vapor deposition (PVD) (or sputtering), chemical vapor deposition (CVD), atomic layer deposition (ALD), or combinations thereof. Other manufacturing techniques to form the aluminum interconnect may include photolithography processing and etching to pattern the conductive materials for vertical connection (for example, vias/contacts 68) and horizontal connection (for example, conductive lines 66). Alternatively, a copper multilayer interconnect may be used to form the metal patterns. The copper interconnect structure may include copper, copper alloy, titanium, titanium nitride, tantalum, tantalum nitride, tungsten, polysilicon, metal silicide, or combinations thereof. The copper interconnect structure may be formed by a technique including CVD, sputtering, plating, or other suitable processes.

Still referring to FIG. 2, a buffer layer 70 is formed over the front side 34 of the interconnect structure 80. In the present embodiment, the buffer layer 70 includes a dielectric material such as silicon oxide (SiO_2). Alternatively, the buffer layer 70 may optionally include silicon nitride (SiN). The buffer layer 70 may be formed by CVD, PVD, or other suitable techniques. The buffer layer 70 is planarized to form a smooth surface by a CMP process.

Thereafter, a carrier substrate 80 is bonded with the device substrate 40 through the buffer layer 100 and the interconnect structure 65, so that processing of the back side 36 of the device substrate 32 can be performed. The carrier substrate 80 in the present embodiment is similar to the device substrate 32 and includes a silicon material. Alternatively, the carrier substrate 80 may include a glass substrate or another suitable material. The carrier substrate 80 may be bonded to the device substrate 32 by molecular forces—a technique known as direct bonding or optical fusion bonding—or by other bonding techniques known in the art, such as metal diffusion or anodic bonding.

Among other things, the buffer layer 70 provides electrical isolation between the device substrate 32 and the carrier substrate 80. The carrier substrate 80 provides protection for the various features formed on the front side 34 of the device substrate 32, such as the pixels 40-42 formed therein. The